REMARKS

Claims 1-12 are pending in the present Application. Claims 2 and 7 have been canceled, Claims 1, 6, and 11 have been amended, and Claims 13-16 have been added, leaving Claims 1, 3-6, and 8-16 for consideration upon entry of the present Amendment.

Support for the amendment to Claim 1 can at least be found in originally filed Claim 2.

Support for the amendment to Claims 6 and 11 can at least be found in originally filed Claim 7.

Support for new Claims 13-16 can at least be found in the specification at paragraphs [0064] to [0065].

No new matter has been introduced by these amendments. Reconsideration and allowance of the claims are respectfully requested in view of the above amendments and the following remarks.

Claim Rejections Under 35 U.S.C. § 102(b)

Claims 1, 2, and 5 stand rejected under 35 U.S.C. § 102(b), as allegedly anticipated by U.S. Patent No. 6,133,074 to Ishida et al. ("Ishida"). Applicants respectfully traverse this rejection.

To anticipate a claim, a reference must disclose each and every element of the claim. *Lewmar Marine v. Varient Inc.*, 3 U.S.P.Q.2d 1766 (Fed. Cir. 1987).

Independent Claim 1 is directed to a method for manufacturing a semiconductor device comprising, *inter alia*, forming a metal layer over a partial region of a transparent substrate; forming a buffer layer covering the metal layer; forming an amorphous semiconductor film above the buffer layer so that the amorphous semiconductor film at least partially overlaps the formation region of the metal layer with the buffer layer therebetween; polycrystallizing the amorphous semiconductor film through laser annealing to form a polycrystalline semiconductor film; and wherein the buffer layer alleviates thermal leakage caused by thermal conduction in the metal layer during polycrystallization of the amorphous semiconductor film through laser annealing.

Ishida discloses a transistor comprising a bottom gate structure in which a gate insulating film is formed covering a metal layer, which is the gate electrode, and a silicon layer formed on the gate insulating film that is polycrystallized through laser annealing. Further, the metal layer 11 of Ishida, which is pointed out by the Examiner, is a gate electrode of the transistor and the structure pointed out by the Examiner as the buffer layer 80 is a gate insulating film.

In Applicants' claimed invention, the layer formed between the metal layer and the semiconductor layer is a "buffer layer", more specifically a layer having a function to alleviate themeral leakage caused by thermal conduction in the metal layer during polycrystallization of the amorphous semiconductor film through laser annealing, and is not a "gate insulating film." The "buffer layer" claimed by Applicants and the "gate insulating film" of Ishida differ from each other not merely in their name, but fundamentally in their functions. More particularly, absent in Ishida, either expressly or inherently, is the teaching that "gate insulating film" can perform a function to alleviate leakage caused by thermal conduction in the metal layer during polycrystallization of the amorphous semiconductor film through laser annealing.

Furthermore, it is noted that Ishida describes in Fig. 3 and related description that the grain sizes of polycrystalline silicon differ from each other in a semiconductor region positioned above a tapered section 76b of the gate electrode 76 and in a semiconductor region positioned above a flat section 76a of the gate electrode 76 (Col. 3, lines 33-57). In addition, Ishida describes a spin on glass (SOG) film that is made of a completely different material and is separately formed between the gate electrode 11 for resolving this problem. Therefore, in Ishida, the gate insulating film formed between the gate electrode, which is the metal layer, and the semiconductor film does not have the thermal leakage alleviation function and Ishida does not teach or suggest a configuration of the gate insulating film having such a function. Since Ishida at least fails to teach a "buffer layer" that can alleviate leakage caused by thermal conduction in the metal layer during polycrystallization of the amorphous semiconductor film through laser annealing, Ishida fails to teach each and every element of Applicants' independent Claim 1. Accordingly, independent Claim 1 is not anticipated by and is

allowable over Ishida. Moreover, as a dependent claim from an allowable independent claim, Claims 2 and 5, are, by definition, also allowable.

Claim Rejections Under 35 U.S.C. § 103(a)

Claims 3-4 stand rejected under 35 U.S.C. § 103(a), as allegedly unpatentable over Ishida. Applicants respectfully traverse this rejection.

For an obviousness rejection to be proper, the Examiner must meet the burden of establishing a *prima facie* case of obviousness, i.e., that all elements of the invention are disclosed in the prior art; that the prior art relied upon, coupled with knowledge generally available in the art at the time of the invention, contain some suggestion or incentive that would have motivated the skilled artisan to modify a reference or combined references; and that the proposed modification of the prior art had a reasonable expectation of success, determined from the vantage point of the skilled artisan at the time the invention was made. *In re Fine*, 5 U.S.P.Q.2d 1596, 1598 (Fed. Cir. 1988); *In Re Wilson*, 165 U.S.P.Q. 494, 496 (C.C.P.A. 1970); *Amgen v. Chugai Pharmaceuticals Co.*, 927 U.S.P.Q.2d, 1016, 1023 (Fed. Cir. 1996).

It is briefly noted that Claims 3-4 are allowable for at least the reason that they depend from an allowable independent claim. More particularly, absent in Ishida is any teaching or suggestion that their "gate insulating film" can act as a "buffer layer" to alleviate leakage caused by thermal conduction in the metal layer during polycrystallization of the amorphous semiconductor film through laser annealing. Accordingly, independent Claim 1 is not obvious and is allowable over Ishida.

Additionally, the thickness of the silicon nitride film and the silicon oxide film forming the buffer layer as claimed in Claims 3 and 4 are not a thickness that would traditionally be employed for the "gate insulating film" or the like in Ishida nor a thickness that would be suggested by Ishida. More specifically, when the gate insulating film is thickened, an operation voltage of the transistor is increased.

As an example, if a thickness of the buffer layer as claimed in Claims 3, 4 (e.g., a total thickness exceeding 200 nm such as (a) a silicon nitride film of approximately 50 nm and a

silicon oxide film of 200 nm or greater and (b) a silicon nitride film of 100 nm or greater and a silicon oxide film of 130 nm or greater is employed), were employed in Ishida, the operation voltage of the thin film transistor of Ishida would become too high and only an unrealistic transistor can be obtained.

When, on the other hand, a thin film is formed as the gate insulating film, unlike the buffer layer of Claims 3-4, it is not possible to alleviate thermal leakage caused by the thermal conduction of the metal layer below the gate insulating film. It is common knowledge for a person skilled in the art to not thicken the gate insulating film of the thin film transistor. Since there is not suggestion in Ishida to thicken the gate insulating film of the film transistor, a person with ordinary skill in the art would not have found it obvious to let the gate insulating film function as an alleviating layer of thermal leakage. Accordingly, dependent Claims 3-4 are not obvious and are allowable over Ishida.

Claims 6-12 stand rejected under 35 U.S.C. § 103(a), as allegedly unpatentable over U.S. Patent No. 6,573,955 to Murade in view of Ishida. Applicants respectfully traverse this rejection.

Applicants' independent Claims 6 and 11 each comprise, *inter alia*, a buffer layer, wherein the buffer layer alleviates thermal leakage caused by thermal conduction in the metal layer during polycrystallization of the first and second amorphous semiconductor films through laser annealing.

In Murade, the polycrystallization of the TFT semiconductor film is achieved not through laser annealing, but through thermal annealing at a high temperature of 600°C to 700°C in a non-oxidizing atmosphere (Col. 11, lines 1-4). Therefore, it is clear that Murade fails to recognize the thermal leakage during the laser annealing process. Additionally, while Ishida recognizes the thermal leakage, Ishida fails to disclose or even suggest a buffer layer between the metal film and the semiconductor film to alleviate the thermal leakage caused by thermal conduction in the metal layer during polycrystallization of the amorphous semiconductor film through laser annealing to the buffer layer. In other words, even if Murade were combined with Ishida, the combined references would still fail to teach or

suggest each and every element of Applicants' independent Claims 6 and 11. Accordingly, independent Claims 6 and 11 are not obvious and are allowable over Murade in view of Ishida. Moreover, as dependent claims from an allowable independent claim, Claims 5-10, and 12 are, by definition, also allowable.

Additionally, with regards to dependent Claims 8-9, Applicants respectfully direct the Examiner's attention to the above arguments with regards to Claims 3-4. Additionally, it is noted, that Murade does not cure the deficiencies of Ishida. More particularly, Murade does not teach or suggest a total thickness exceeding 200 nm such as (a) a silicon nitride film of approximately 50 nm and a silicon oxide film of 200 nm or greater and (b) a silicon nitride film of 100 nm or greater and a silicon oxide film of 130 nm or greater. Accordingly, dependent Claims 8-9 are further non-obvious and are allowable over Murade in view of Ishida.

It is believed that the foregoing amendments and remarks fully comply with the Office Action and that the claims herein should now be allowable to Applicants. Accordingly, reconsideration and allowance are requested.

If there are any additional charges with respect to this Amendment or otherwise, please charge them to Deposit Account No. 06-1130.

Respectfully submitted,

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